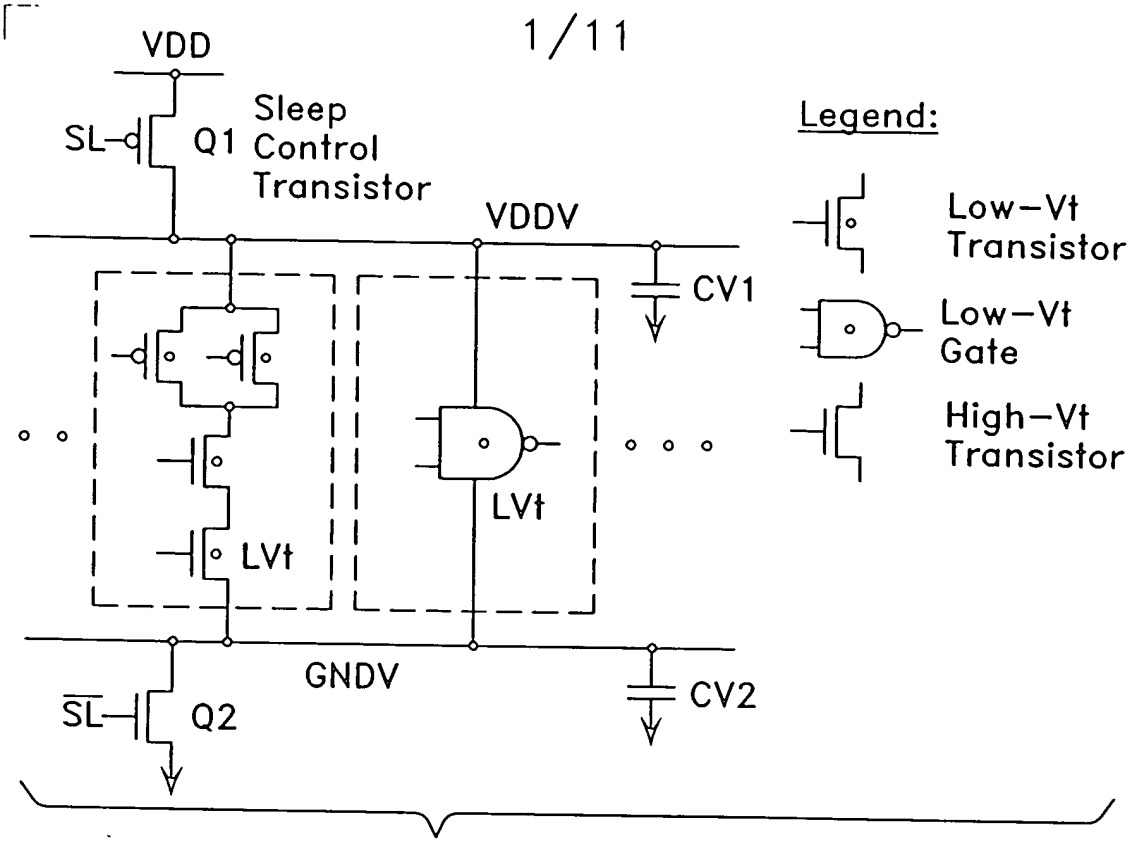


Fig. 1 (PRIOR ART)

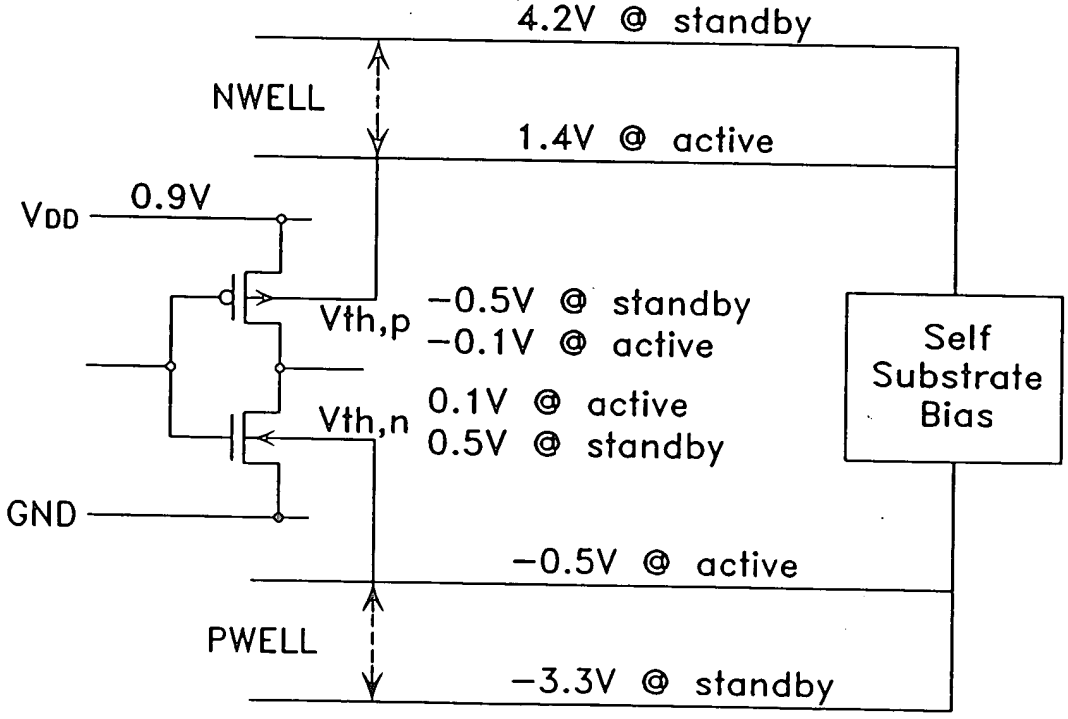


Fig. 2 (PRIOR ART)

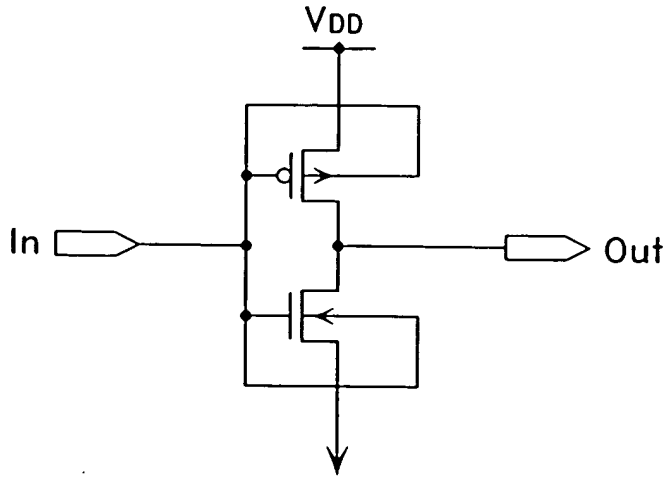
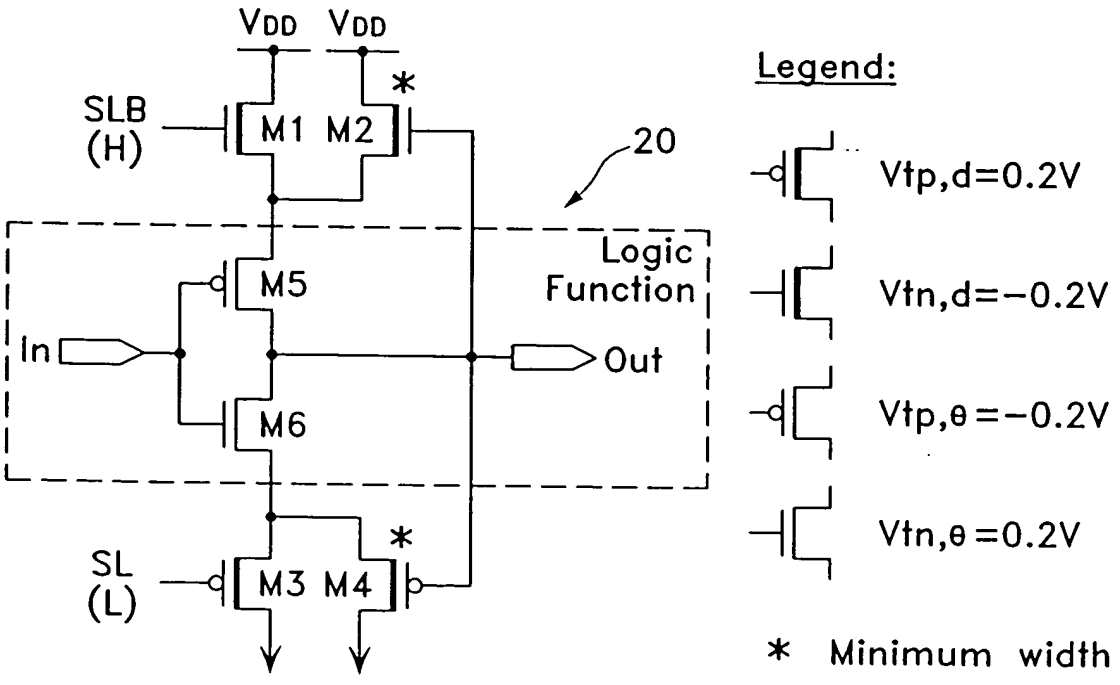
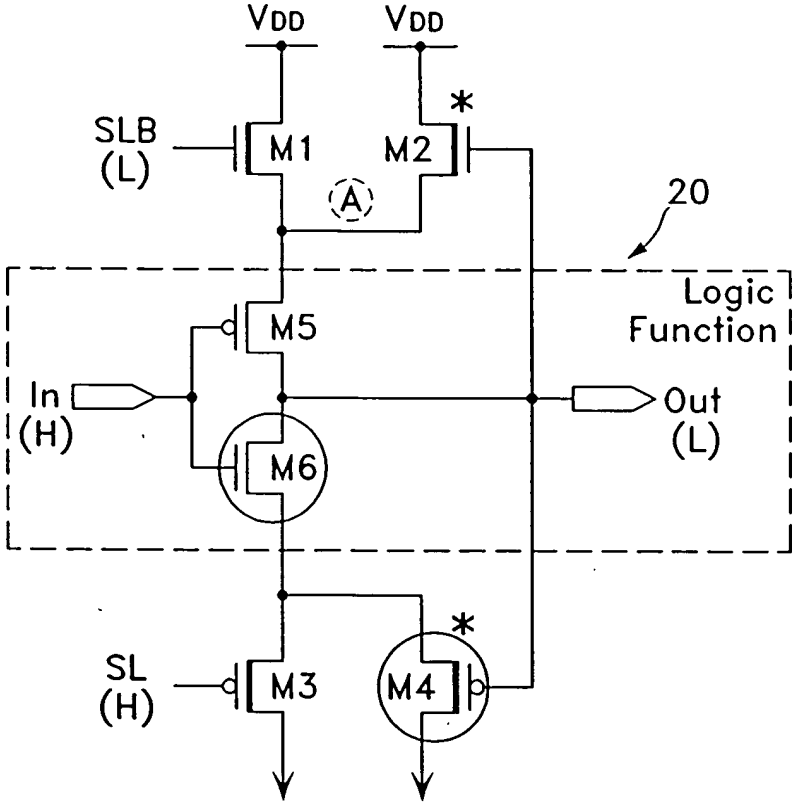


Fig. 3 (PRIOR ART)

Fig. 4





Legend:
* Minimum width

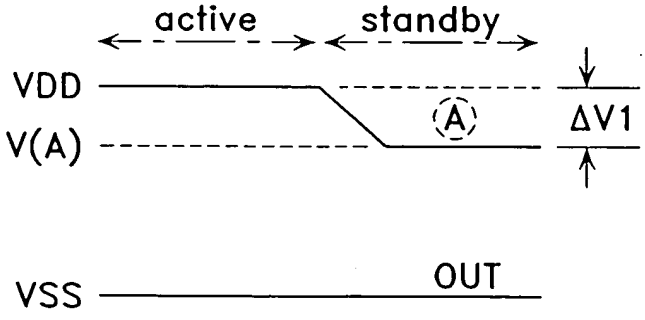


Fig. 5

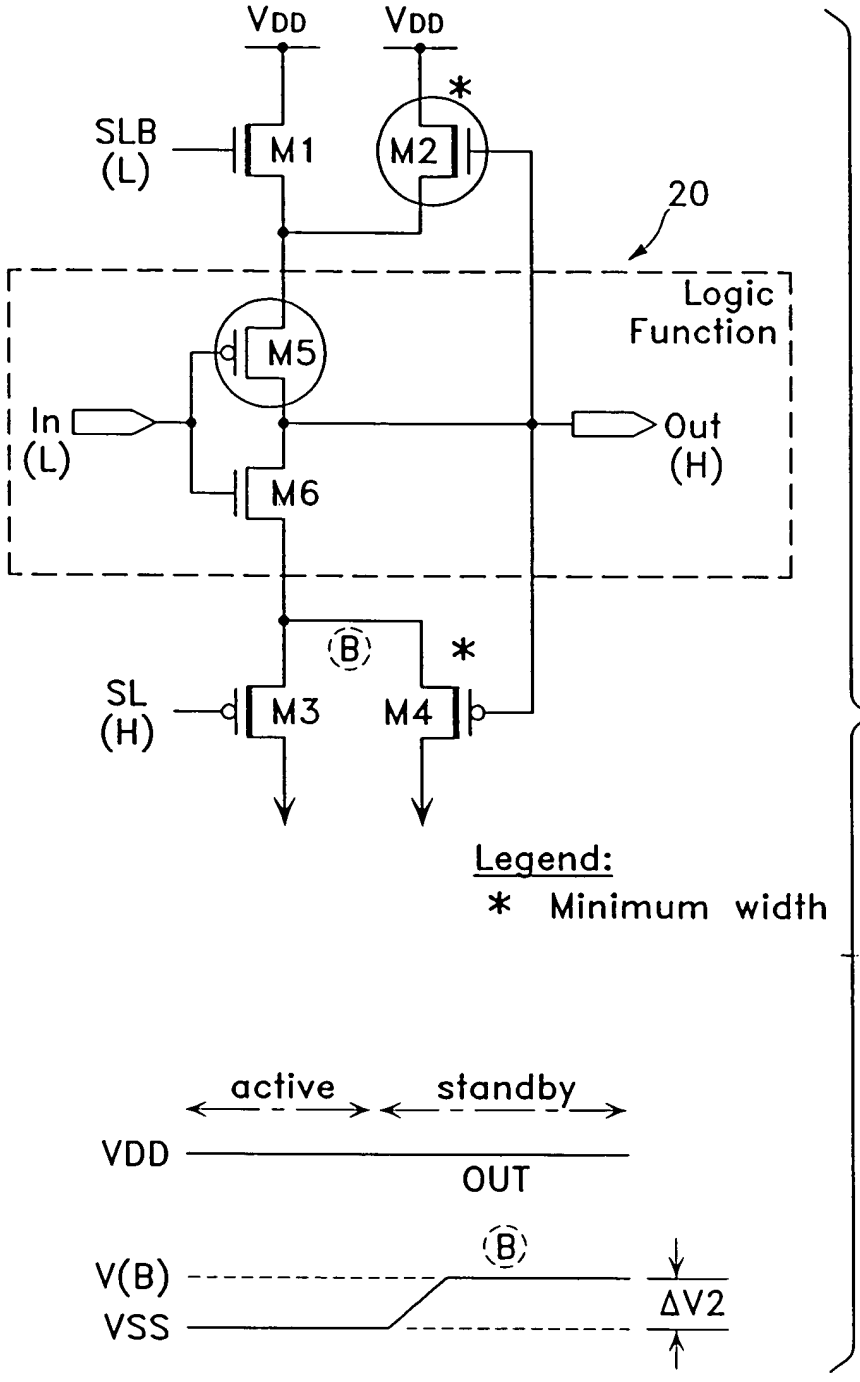

VDD
VDD
*
SLB
(L)
M1
M2
20
Logic
Function
M5
In
(L)
Out
(H)
M6
B
*
SL
(H)
M3
M4
Legend:
* Minimum width
active
standby
VDD
OUT
B
V(B)
VSS
ΔV2

Fig. 6

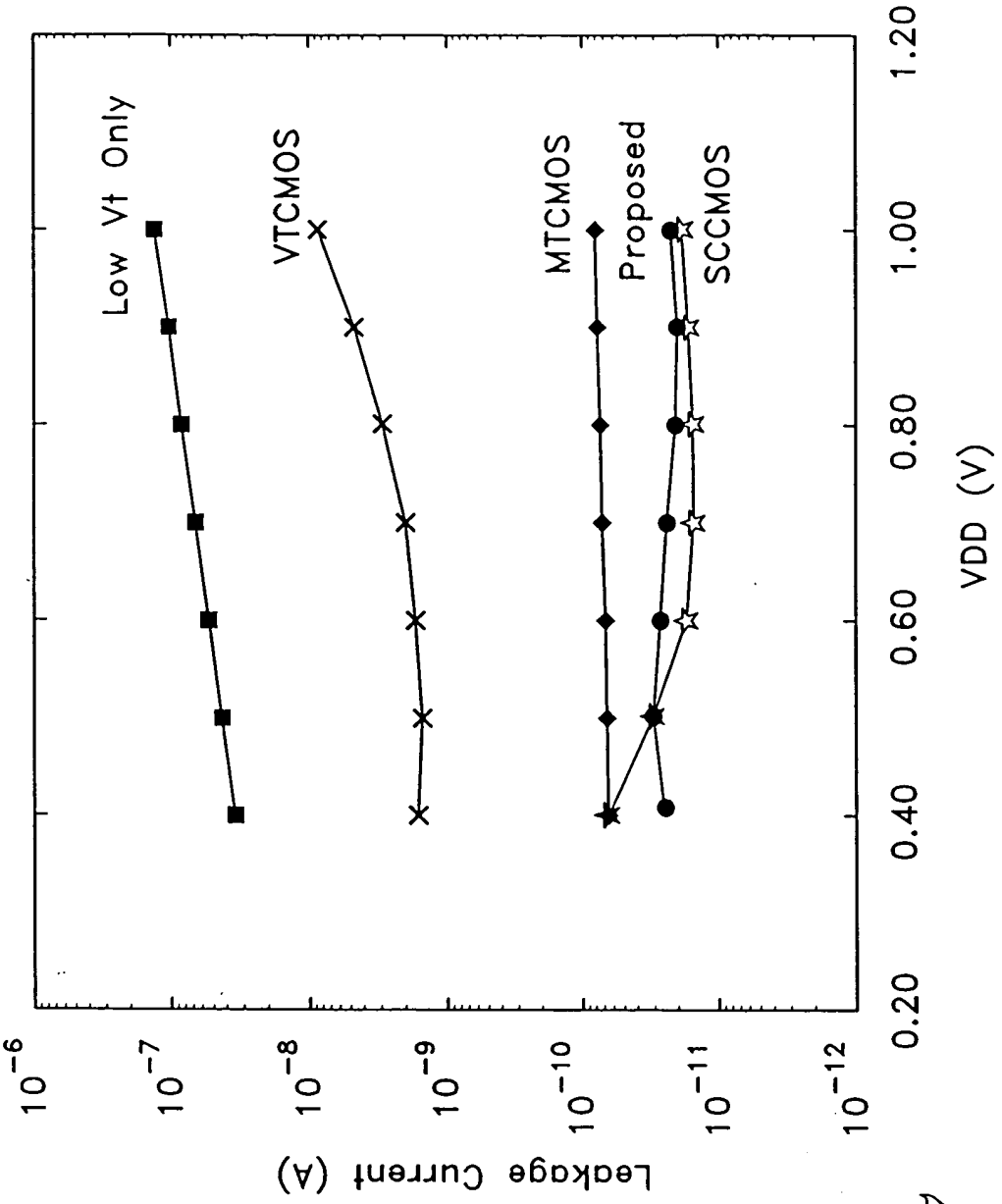

Low Vt Only
VTCMOS
MTCMOS
Proposed
SCCMOS
Leakage Current (A)
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
0.20
0.40
0.60
0.80
1.00
1.20
VDD (V)

Fig. 7

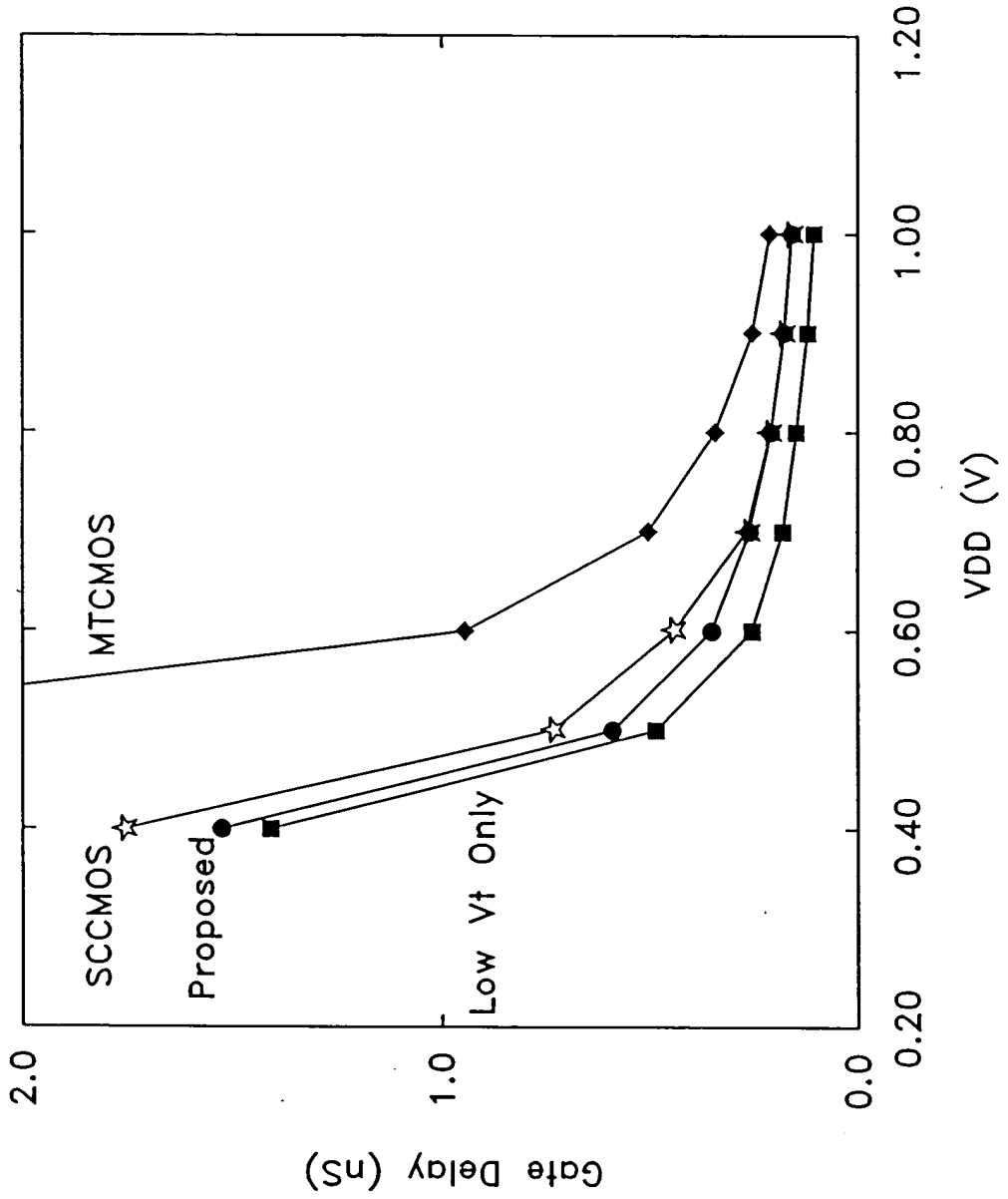

MTCMOS
SCCMOS
Proposed
Low Vt Only
2.0
1.0
0.0
Gate Delay (nS)
0.20
0.40
0.60
0.80
1.00
1.20
VDD (V)

Fig. 8

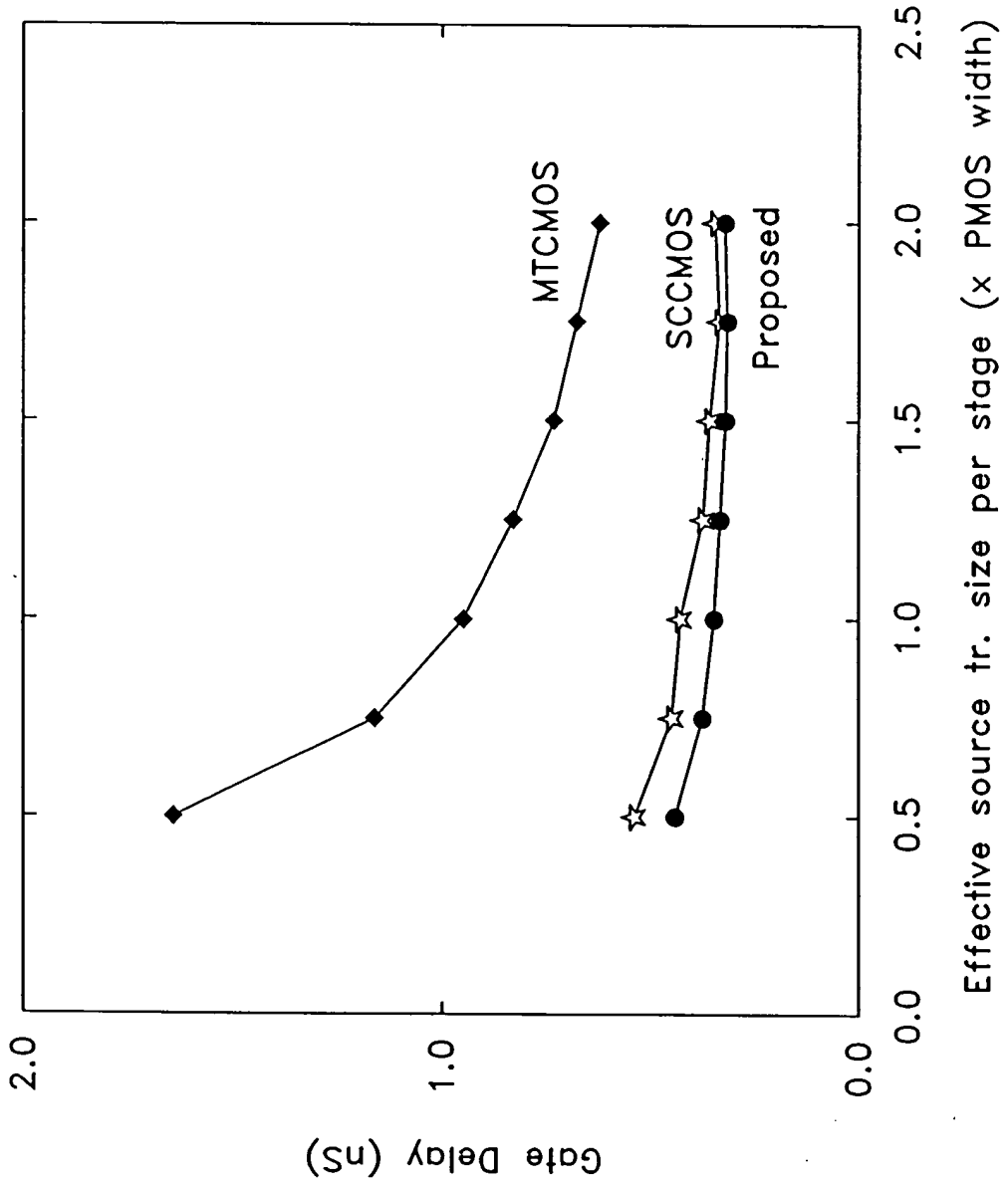

Gate Delay (nS)
2.0
1.0
0.0
0.0
0.5
1.0
1.5
2.0
2.5
Effective source tr. size per stage (x PMOS width)
MTCMOS
SCCMOS
Proposed

Fig. 9

8/11

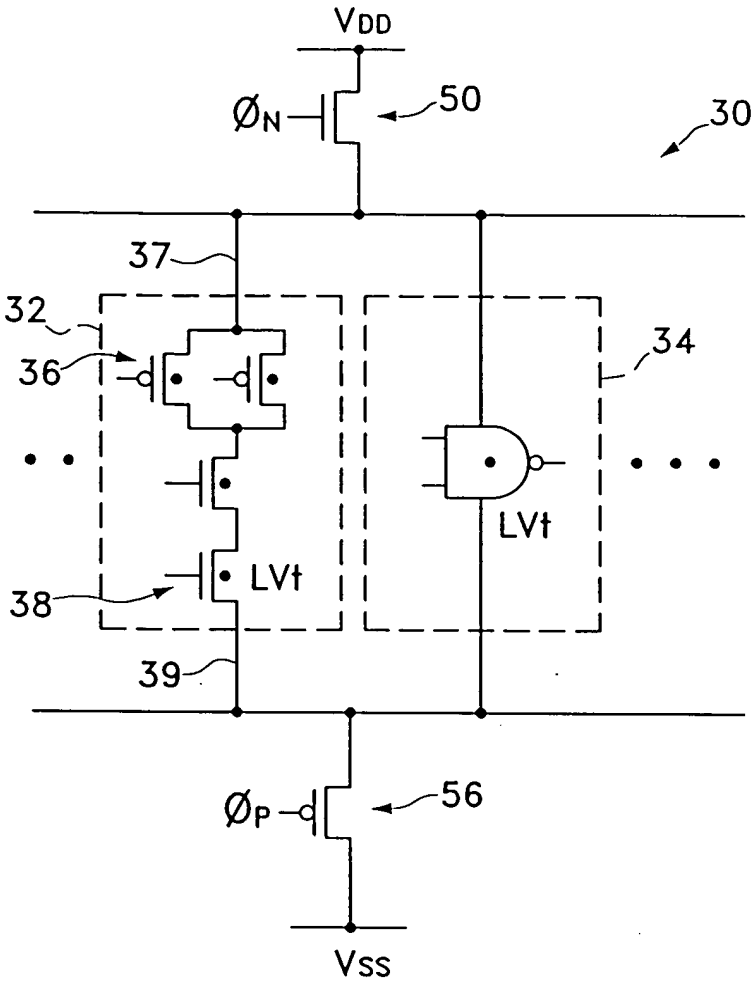


Fig. 10

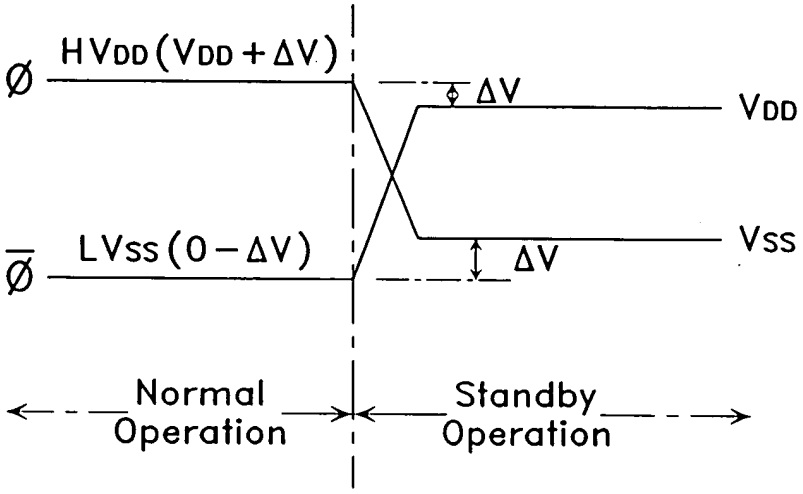


Fig. 11

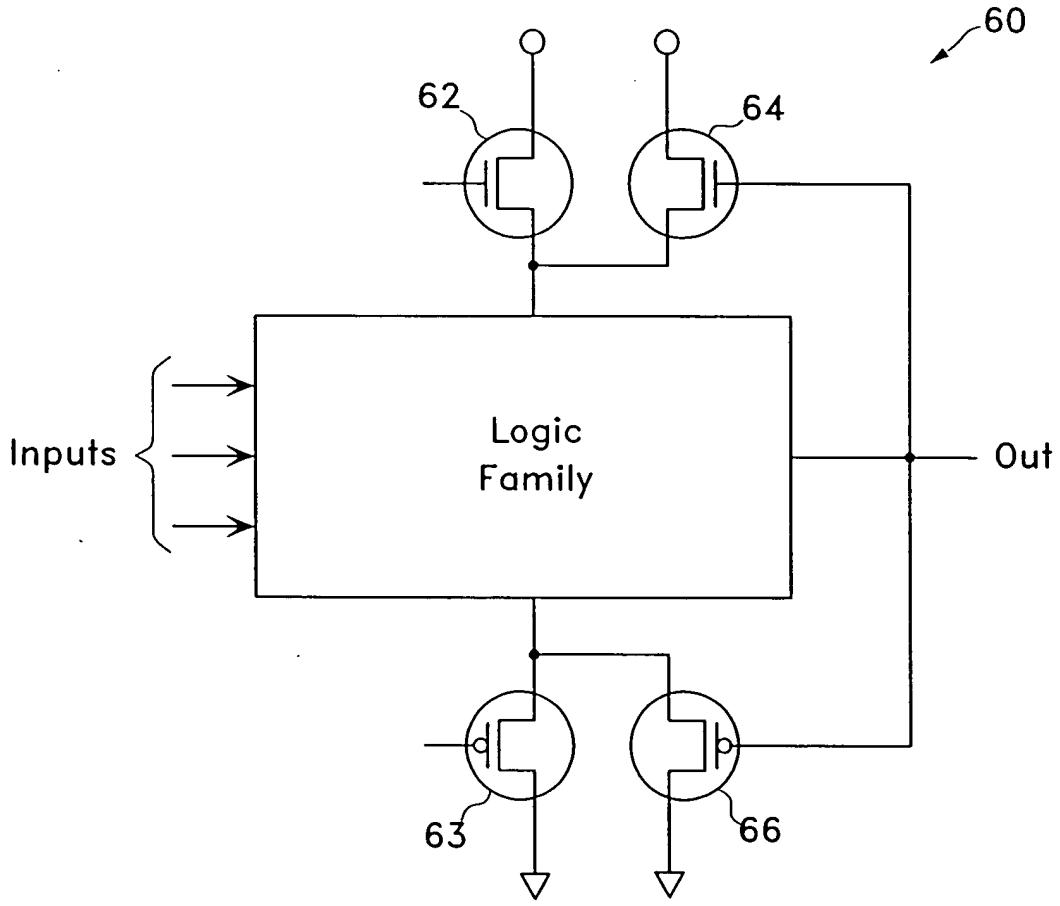


Fig. 12

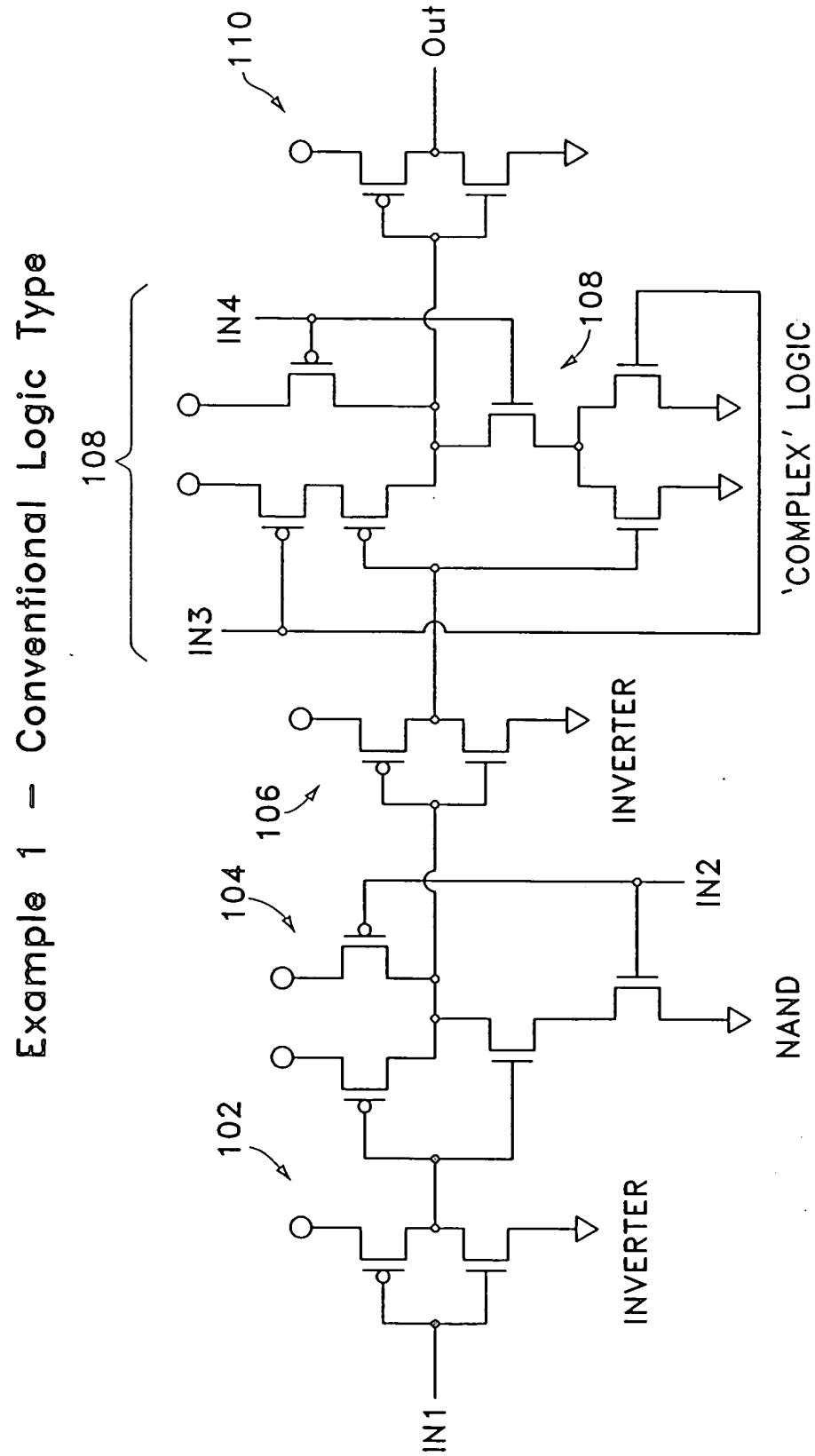


Fig. 13 (PRIOR ART)

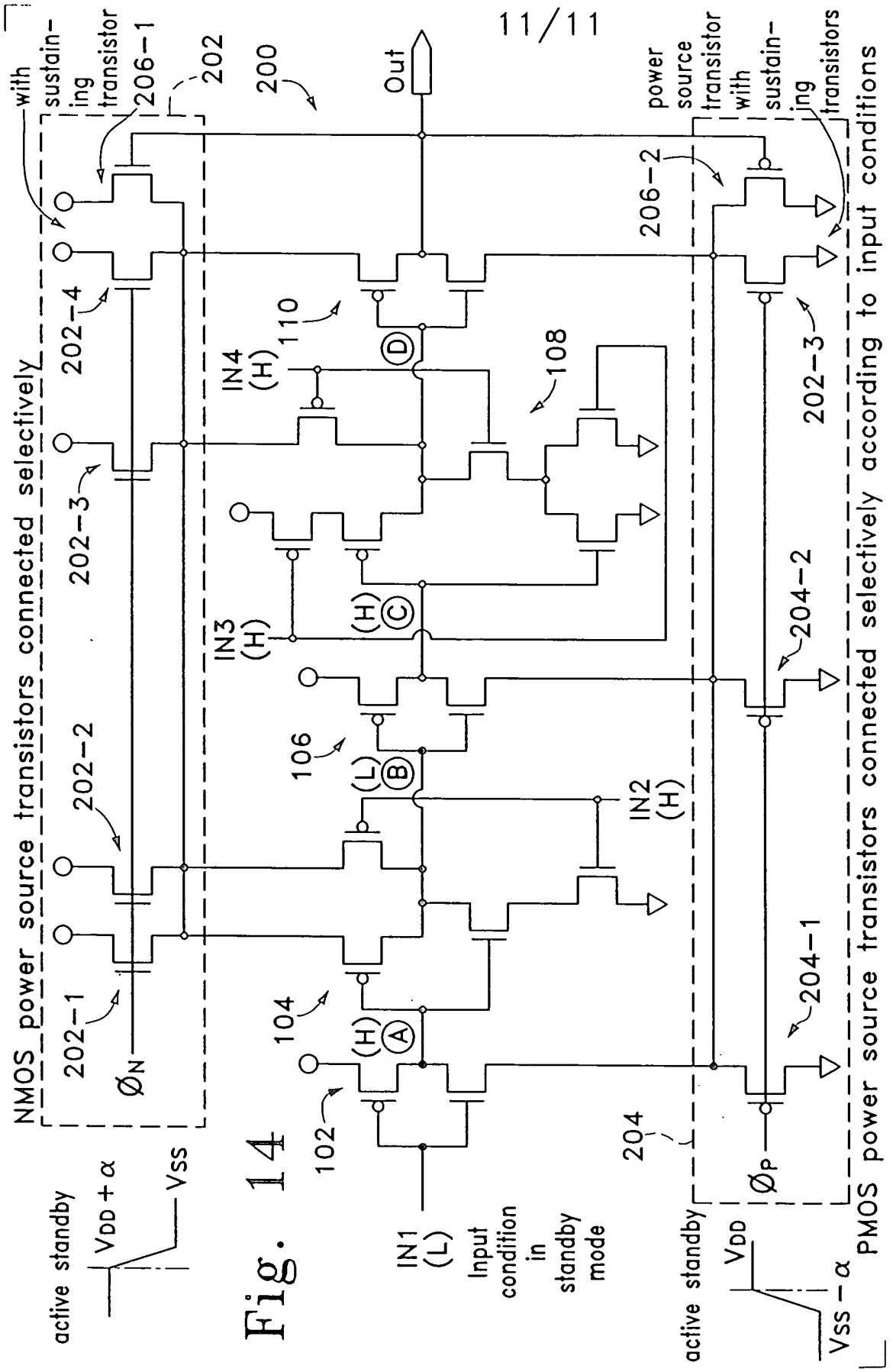

NMOS power source transistors connected selectively
PMOS power source transistors connected selectively according to input conditions
with sustaining transistor 206-1
power source transistor with sustaining transistors
202
200
Out
206-2
202-4
202-3
202-2
202-1
204-2
204-1
204
108
110
106
104
102
IN1 (L)
IN2 (H)
IN3 (H)
IN4 (H)
(A) (H)
(B) (L)
(C) (H)
(D)
ϕ_N
ϕ_P
active standby
$V_{DD}+\alpha$
Vss
active standby
V_{DD}
$V_{SS}-\alpha$
Input condition in standby mode

Fig. 14